Docket No.: 2003P12591

# CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of PCT/EP2005/050050, filed with the European Patent Office on January 7, 2005.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Hollywood, Florida

Rebekka Pierre

August 2, 2006

Lerner Greenberg Stemer LLP
P.O. Box 2480
Hollywood, FL 33022-2480
Tel.: (954) 925-1100
Fax.: (954) 925-1101

Description

Device and method for equalizing the charge of serially connected capacitors belonging to a double layer capacitor

The invention relates to a device for equalizing the charge of the serially connected capacitors belonging to a double layer capacitor, particularly in a motor vehicle electrical system, according to Claim 1 or 2.

The invention also relates to a method for operating this device according to Claim 5.

Double layer capacitors have proved to be the most favorable technical solution for the storage and delivery of short-term high power levels in a motor vehicle electrical system, for example with regard to acceleration support (boosting) for the internal combustion engine by means of an integrated starter/generator functioning as an electric motor or to the conversion of kinetic energy into electrical energy during the regenerative braking process (recuperation) by means of an integrated starter/generator functioning as a generator.

The maximum voltage of a single capacitor of a double layer capacitor is limited to about 2.5V to 3.0V, with the result that for a voltage of for example 60V - a typical voltage value for a double layer capacitor used in a 42V vehicle electrical system - about 20 to 25 single capacitors need to be serially connected to form a capacitor stack.

Dependent on the differences in the spontaneous discharge of the single capacitors (in the region of about 5% to 8% within 16 hours), a charge imbalance builds up in the capacitor

stack over the course of time which ultimately renders the double layer capacitor unusable unless a charge equalization is performed. If the discharge curve is extrapolated to periods of weeks and months, which are relevant in the case of motor vehicles, then the existing problem becomes obvious.

It is not however possible to perform a simple charge equalization for a double layer capacitor, for example by slightly overcharging the stack as in the case of a lead-acid accumulator.

With regard to a large number of serially connected accumulators, a method is known from EP 0 432 639 B2 for performing a charge equalization between a weakly charged accumulator and the group of remaining accumulators by providing for each individual accumulator in the accumulator stack a comparator circuit and a charging circuit, which includes a squarewave function generator, and also a diode, a transformer and a contact breaker. By means of this device functioning as a flyback converter (using the isolating transformer principle), energy is removed from the entire stack and this is subsequently fed back into the most discharged accumulator.

This effort may be justified for two or three accumulators, but it is decidedly too high for a stack comprising twenty or more accumulators/capacitors.

The object of the invention is to create a device having a simplified structure which can be used to achieve self-controlled operation for charge equalization between the single capacitors in the capacitor stack of a double layer capacitor with limited engineering effort. The object of the

invention is also to specify a method for operating this device which enables functional monitoring of the device and of the capacitor stack to be performed.

This object is achieved according to the invention by a device according to the features described in Claim 1 or 2 and a method according to the features described in Claim 5.

Advantageous developments of the invention are set down in the subclaims.

Embodiments according to the invention will be described in detail in the following with reference to a schematic drawing. In the drawings:

Figure 1 shows the circuit of a first embodiment according to the invention,
Figure 2 shows voltage waveforms for selected points of this circuit,
Figure 3 shows current waveforms for selected points of this circuit,
Figure 4 shows the circuit of a second embodiment of the invention.

Figure 1 shows the circuit of a first embodiment according to the invention with a double layer capacitor DLC having one positive and one negative terminal V+ and V-, and consisting of n serially connected single capacitors C1 to Cn.

The circuit has a flyback transformer Tr0 whose primary and secondary windings are wound in phase opposition to one another and which has the function of a magnetic energy store. The spots drawn in for the transformers in Figures 1

and 4 denote the respective start of the winding.

The primary winding of the flyback transformers Tr0 is connected on the one hand to the positive terminal V+ and on the other hand to the drain terminal of a switching transistor T1 taking the form for example of a MOSFET. The switching transistor T1 can however also take the form of a bipolar transistor with base, emitter and collector terminals. The source terminal of the switching transistor T1 is connected on the one hand to the inverting input of a first voltage comparator KOMP1 and on the other hand by way of a first resistor R1 to the negative terminal V- which is at the reference potential (ground) of the circuit.

The gate terminal of the switching transistor T1 is connected to the output of a first AND element UND1, to whose one input a control signal EN which is supplied by an external control logic circuit that is not shown is fed, and whose other input is connected to the output of a second AND element UND2.

The noninverting input of the first voltage comparator KOMP1 is connected to a single-ended reference voltage Vref1 and its output is connected to an input of the second AND element UND2 and to a first input of a monitoring unit DIAG (diagnosis).

One terminal of the secondary winding of the flyback transformer Tr0 is connected directly, the other terminal by way of a first diode D0 and a second resistor R2, to the negative terminal V-. A first capacitor C0 is connected on the one hand to the cathode of the first diode D0 and on the other hand to the negative terminal V-. The connection point of the cathode of the first diode D0 and the second resistor

R2 is connected to the inverting input of a second voltage comparator KOMP2, whereas the reference voltage Vref1 is applied to the latter's noninverting input.

The output of the second voltage comparator KOMP2 is connected on the one hand to the other input of the second AND element UND2 and on the other hand to a second input of the monitoring unit DIAG.

A third input of the monitoring unit DIAG is connected to the inverting input of the second voltage comparator KOMP2 and a second single-ended reference voltage Vref2 is applied to a fourth input of the monitoring unit DIAG. The output of the monitoring unit DIAG delivers a status signal ST which is monitored by an external evaluation logic circuit, not shown, which will be described in detail later.

Each single capacitor C1 to Cn of the double layer capacitor DLC is assigned a single transformer Tr1 to Trn which is wound in-phase (primary and secondary windings are wound in-phase with respect to one another).

The start of winding of the secondary winding of each single transformer Tr1 to Trn is connected by way of a single diode D1 to Dn to the positive terminal +C1 to +Cn of the single capacitor C1 to Cn associated with it, while the other terminal is connected directly to the other (negative) terminal of the single capacitor C1 to Cn associated with it.

The primary windings of the single transformers Tr1 to Trn are connected in parallel, whereby the common start of winding is connected to the cathode of the first diode D0 and the common end of winding is connected to negative terminal

V- (reference potential) and to the end of winding of the secondary winding of the flyback transformer Tr0. In this situation, the connection between the flyback transformer (Tr0) and the single transformers is implemented by means of a two-wire bus cable.

The method for operating this device is described in the following with reference to signal waveforms illustrated in Figures 2a to 2e (voltages) and also 3a and 3b (currents) for selected points of the circuit. It is assumed in this situation that the nominal voltage of the double layer capacitor DLC = 10V, and the nominal voltage of a single capacitor = 2.5V, where n = 4. A charge equalization takes place here from the overall voltage of the double layer capacitor DLC, but can also take place from other energy storage devices as soon as any such are connected to the double layer capacitor DLC, which is not however shown in Figure 1.

By means of the aforementioned control signal EN (Figure 2a, start at point in time t = 1µs), for the duration of the latter the switching transistor T1 is released by way of the AND element UND1 (Figure 2b shows the voltage at the drain terminal of the switching transistor T1; up to point in time t = 1µs the voltage at the drain terminal is +10V, at point in time t = 1µs it drops to approximately 0V). If the control signal EN and the output of the AND element UND2 are High level, then switching transistor T1 is made conducting (Figure 2e, t = 1µs).

A current begins to flow from the positive terminal V+ through the primary winding of the flyback transformers Tr0, through the switching transistor T1 and the first resistor R1

to the negative terminal V- (Figure 3a), whereby a voltage proportional to this current is present at the first resistor R1 (Figure 2c).

The voltage present at the first resistor R1 rises as the current flow increases, in other words also as charging of the core of the flyback transformer Tr0 increases. If it reaches the value of the reference voltage Vref1 at point in time t ≅ 2.2µs, then the voltage comparator KOMP1 switches its output from High to Low level, whereupon the output of the AND element UND" likewise goes to Low level and thus makes the switching transistor nonconducting. The voltage comparator KOMP1 is thus used for sensing the primary current of the flyback transformer Tr0.

Since the current flowing through the first resistor R1 now drops rapidly, the voltage present at it is also reduced and drops below the value of the reference voltage Vref1. The output from KOMP1 would now immediately return to High level, as a result of which switching transistor T1 would again be made conducting.

In order to prevent this, the voltage jump occurring on the secondary side when switching off the flyback transformer Tr0 is detected and used in order to keep switching transistor T1 nonconducting until the flyback transformer Tr0 has been completely discharged.

When the switching transistor T1 is made nonconducting, the voltage of the primary side of the flyback transformer Tr0 rises - driven by the energy stored in its core - beyond the voltage at the positive terminal V+. The voltage at its secondary side rises likewise; the current caused by it flows

by way of the first diode D0 operated in the forward direction (Figure 2d) and at the second resistor R2 generates a proportional voltage whose rate of rise is determined by the charging of the first capacitor C0. This voltage reaches the inverting input of the voltage comparator KOMP2. The latter is thus used for sensing the secondary voltage of the flyback transformer Tr0.

As long as this voltage is greater than the reference voltage Vref1, the output from the voltage comparator KOMP2 switches to Low level, such that switching transistor T1 remains nonconducting by way of the AND elements UND2 and UND1. Only when the flyback transformer Tr0 is completely discharged and the voltage breaks down on its secondary side does the voltage at the inverting input of the voltage comparator KOMP2 drop below the reference voltage Vref1, whereupon its output goes to High level and makes the switching transistor T1 conducting again by way of the AND elements UND2 and UND1.

The fact that the voltage at the secondary winding of the flyback transformer Tr0 becomes negative when the switching transistor T1 is made conducting is unimportant in this situation because the first diode D0 is now blocking.

After the switching transistor T1 is made nonconducting, the energy stored in the flyback transformer Tr0 flows by way of the secondary winding of the flyback transformer Tr0 and the first diode D0 to the first capacitor C0 and to the parallel-connected primary windings of the small single transformers Tr1 to Trn and thence by way of their secondary windings and also the single diodes D1 to Dn to the single capacitors C1 to Cn.

The rapid current rise in the secondary winding of the flyback transformer Tr0 associated with making the switching transistor T1 nonconducting initially charges the first capacitor C0. By this means, the magnetizing inductances of the single transformers Tr1 to Trn receive sufficient time to build up current such that a current can ultimately also flow on their secondary sides.

On the secondary side of a single transformer, Tr1 for example, a voltage is thus produced which corresponds to the sum of the charging voltage of the single capacitor C1 and the forward voltage of the single diode D1. This is also the case in the same manner for the secondary voltages of the transformers Tr2 to Trn. A typical value for this voltage is for example 3.2V, whereby the charging voltage of C1 is 2.5V and the forward voltage of D1 is 0.7V. When Schottky diodes are used, the diode forward voltage is only about 0.3V.

The primary voltage of each single transformer is given by the respective secondary voltage and the transformation ratio - which is set to be identical for each single transformer Tr1 to Trn.

It follows from this that different primary voltages for the transformers Tr1 to Trn also result for different charging voltages of the single capacitors C1 to Cn.

However, since the primary windings of all the transformers Tr1 to Trn are now connected in parallel, this necessarily results in a uniform primary voltage - and thus also a uniform secondary voltage.

In this situation, this uniform primary voltage is caused by

the single capacitor, C1 for example, having the lowest charging voltage because the latter actually also produces the lowest primary voltage at the single transformer Tr1 assigned to it.

This uniform primary voltage is also present - transformed with the reciprocal transformation ratio of the transformers - at the secondary sides of all the other transformers Tr2 to Trn.

However, since this voltage is now lower than the sum of the charging voltage of the respective single capacitor C2 to Cn and the forward voltage of the assigned single diode, these single diodes D2 to Dn will not conduct and the single capacitors C2 to Cn receive no charging current. Rather, the current coming from the secondary side of the flyback transformer Tr0 essentially flows to the single capacitor (C1) with the lowest voltage as a charging current.

During the course of the charging process the voltage of this capacitor will now rise and it reaches the value of the capacitor with the second lowest voltage. From this point on the single diode assigned to this capacitor also becomes conducting and this capacitor too receives a part of the charging current. Therefore, from this point on the voltages of both capacitors will rise until their voltage reaches the value of the capacitor with the third lowest voltage, etc.

This process is repeated until all the capacitors C1 to Cn in the stack ultimately have the same voltage. With that, the charging process is then completed.

By means of the monitoring circuit DIAG, the signal duration

= charging time which can be measured at the output of the voltage comparator KOMP1 and the signal duration = discharging time for the flyback transformer Tr0 which can be measured at the output of the voltage comparator KOMP2 are measured and compared with predefined upper and lower limit values.

If the measured times lie within the predefined limit values, then it can be assumed that the double layer capacitor DLC and the charge equalizing circuit are in a perfect state. Faults such as a short circuit or open circuit in individual single capacitors can be easily detected in this manner.

An additional measurement of the rectified secondary voltage of the flyback transformer Tr0 (Figure 2d) furthermore permits detection of the lowest voltage of a single capacitor C1 to Cn by, for example, capturing the amplitude in the timing dimensions according to Figure 2d, approximately 0.2µs to 1.0µs after the rise in the voltage and the transient reaction. This value is proportional to the currently smallest voltage of a single capacitor.

A comparison of this value with predefined upper and lower limit values likewise provides information about the operation of the double layer capacitor DLC.

The overall status of the double layer capacitor DLC captured in this manner is displayed on the output of the monitoring unit DIAG by means of a status signal ST with the corresponding level. This status signal ST indicates whether the double layer capacitor DLC is functioning fault-free or whether a visit to a workshop is required for investigation or repair.

Figure 4 shows the circuit for a second embodiment according to the invention, which is essentially identical to the circuit according to Figure 1, apart from the fact that in it the flyback transformer Tr0 is replaced by an inductor L1 and a transistor T2, for example a PNP transistor, and a third resistor R3, are additionally added.

At the point at which the flyback transformer Tr0 was to be found in Figure 1, the circuit includes an inductor L1. The one terminal of the inductor L1 is connected to the positive terminal V+ and the other terminal is connected on the one hand to the drain terminal of the switching transistor T1 and on the other hand by way of a first diode D0 and a third resistor R3 to the emitter terminal of a transistor T2 operated as a level converter, whose base terminal is connected to the positive terminal V+ and whose collector terminal is connected to the second resistor R2 and the inverting input of the voltage comparator KOMP2. The first capacitor C0 is connected on the one hand to the cathode terminal of the first diode D0 and on the other hand to the positive terminal V+.

The connection between the primary windings of the single transformers Tr1 to Trn and the inductor L1 is implemented such that the interconnected starts of windings are connected to the connection point of first diode D0 and third resistor R3, and that the interconnected ends of windings are connected to the positive terminal V+.

The remainder of the circuit is, as already mentioned, identical to that according to Figure 1. With regard to this embodiment too, the connection between the inductor (L1) and

the single transformers is implemented by means of a two-wire bus cable.

With regard to this circuit, the measurement of the discharging voltage of the inductor L1 must be related to the voltage present at the positive terminal V+, which is done by means of the PNP transistor T2 operated as a level converter.

If switching transistor T1 has been made conducting and its drain voltage is therefore low, then the first diode D0 is blocking and thus prevents a current from flowing from the inductor L1 through the base/emitter diode of transistor T2 in the inverse direction.

Since the base voltage of transistor T2, which is at the potential of the positive terminal V+, is now higher than its emitter voltage, transistor T2 is turned off and the voltage at R2 or at the inverting input of the voltage comparator KOMP2 is 0 volts.

If the voltage at the inductor L1 jumps above the potential at the positive terminal V+ after the switching transistor T1 has become nonconducting, then the first diode D0 is made conducting and a current begins to flow from the inductor L1 by way of the first diode D0, the third resistor R3, transistor T2 and the second resistor R2 to the negative terminal V- (reference potential).

At the second resistor R2 this current generates a positive voltage which, as described in the case of the embodiment according to Figure 1, is higher than the reference voltage Vref1, with the result that the output from the voltage comparator KOMP2 switches to Low level, which ultimately

makes switching transistor T1 nonconducting, by way of the AND elements UND2 and UND1.

Only when the inductor L1 is completely discharged does its discharging voltage drop to almost reference potential, whereupon the current flow through the second resistor R2 breaks down and switching transistor T1, as described in the case of the embodiment according to Figure 1, is made conducting again.

The remainder of the mode of functioning of the circuit and the method for operating the circuit are identical to the case of the embodiment according to Figure 1, as already described further above.